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The Electrical Characteristics of (CdS – CdTe) Structure Thin Films

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ABSTRACT

Thin films of (CdS – CdTe) have been fabricated on glass substrates using vacuum thermal evaporation technique. The effect of substrate temperature on the electrical characteristics for the fabricated structure at (4000 ^{0}A) thickness with 2 ^{0}A / sec deposition rate have been investigated.

The substrate temperature was very important parameter on the fabricated films , and a good adhesion film obtained at (170 ^{0}C). Resistivity of the films decreased as the substrate temperature increased up to (170 ^{0}C) and then started increasing gradually at temperatures above 170 ^{0}C. Also, has been observed that the resistivity decreased with increasing the biasing voltage.

The linear relation for (I –V) characteristics at different substrate temperatures has been obtained for fabricated films.

ألخواص الكهربـائـية لأغشـية (كبريتيد الكادميوم - تلوريد الكادميوم) الرقيقة

الملخص

تم ترسيب نماذج من أغشية رقيقة من (كبريتيد الكادميوم – تلوريد الكـادميوم) علـى شـرائح زجاجية باستخدام تقنية التبخير الحراري الفراغي. وقد بحث تـأثير درجـة حـرارة الأسـاس علـى الخواص الكهربائية لأغشية بسمك (4000 ^{0}A) وبمعدل ترسـيب (2 ^{0}A / sec). إن أهـم العوامـل تأثيراعلى الأغشية المصنعة هـي درجة حرارة الأساس، فلقد حصلنا على أغشية ذات معامل التـصـاق جيد عند درجة حرارة الأسـاس(170 ^{0}C). لقد وجد أن مقاومية الأغشـية تقل مع زيـادة درجـة. حرارة الأسـاس إلى حد (170 ^{0}C) ثم بدأت تزداد تدريجيا عند درجات حرارة أعلى من (170 ^{0}C) وقد لوحظ بأن المقاومية تقل كذلك مع زيادة فولتية التجهيز.

كذلك تم الحصول على علاقة خطية لخواص (تيار – فولتية) للأغشية المصنعة عند درجـات حـرارة أساس مختلفـة.

INTRODUCTION

Cadmium telluride and cadmium sulphide belonging to the (II – VI) group of the periodic table presents various properties (energy gap about 1.5 eV for CdTe , 2.42 eV for CdS , direct fundamental transition, n – type or p – type conductivity , … etc), make them attractive for applications as different as gamma and X – ray detectors and photo voltaic devices (Candless et al., 200) and (Kim and Im, 1990) . For the above features it is necessary to investigate the electrical properties for the (CdS – CdTe) compound . These films (CdS, CdTe) are generally prepared by thermal vacuum evaporation techniques (Nory, 1995) and (Hussain, 1992) .The quality of the films above depends upon; the type of the substrate and cleaning it , rate of deposition, quality of vacuum technique of evaporation , and the substrate temperature (Ferekides et. al., 1993) .

CdS and CdTe thin films are polycrystalline individual crystallite, generally of a good quality each but are interrupted by numerous grain boundaries. The grain boundaries are regions of increased disorder, at which charge trapped, and form potential barriers, that impede carrier transport .

The electrical conductivity is limited by the barriers of grain boundaries. If the voltage drop in the bulk grain is negligible compared with the voltage drop in the barrier , the film resistivity follows the relation (Cuenca and Morenza, 1985) :

$$\rho = \frac{V}{D \cdot J} \quad \text{..... (1)}$$

Where D : is the grain size .
J : is the current density .
V : is the voltage drop in the barrier .

It is a fact that the substrate temperature suitable to obtain the right conductivity are lower than those necessary to obtain large sized grains (Mohammad, 1995). The following properties of (CdS - CdTe) thin films have been studied in some details : dark surface and bulk resistivity as a function of substrate temperature, and (I – V) characteristics.

EXPERIMENTAL WORK

Fabrication of (CdS – CdTe) alloy thin films which obtained by mixing both semiconductors powder in the ratio of 1:1 by weight of thickness (4000 °A) were carried out on a glass substrates using vacuum thermal evaporation technique. An optimum setting was fed to the microcomputer of Balzers system in order to set - up the substrate temperatures, vacuum pressure, deposition rate , and film thickness . Aluminum has been used as a contact layer for both faces . The masks which are used, have been made from aluminum foil with thickness 0.1 mm .After cutting manually the masks with a certain shape (rectangular 4mm * 15mm), these masks together with the aluminum metal which is to be evaporated as a contact layer were subjected to a cleaning cycle. The evaporation conditions of aluminum were as follows: (TH = 2000 °A, R = 5°A/sec, Ts =20 °C & Pr. = 4*10^-6 Torr). More details on the use of the system and the steps followed to reach optimum setting of the system and the cleaning procedures are outlined else where

(Ali, 1989) .The cleaned substrates were fixed inside the chamber, then the evaporation of air was started. after obtaining a vacuum of ($4*10^{-6}$ Torr), the substrates were heated up to 300 °C and maintained at this temperature for two hours for degassing and to improve film adherence , then cooled down to the required temperature which to be kept constant during the deposition process . The prepared films were deposited at (2 °A/sec and TH = 4000 °A) with different substrate temperatures (110 °C – 240 °C).

In order to perform the electrical measurements, silver paste was used to connect device electrodes (Al) with the measuring circuit. a digital multi- meter (data precision 1351) and a keithley (177 microvolt DMM) were used to measure the applied voltage across the sample . The voltage was taken from a stabilized D.C power supply (Farnell – L 30–2) .There was mechanical probes to connect the different electrodes with the measuring units.

X – Ray diffraction technique was used to test the powder and films structure.

RESULTS AND DISCUSSIONS

The variation of bulk resistivity with the substrate temperature is measured for different biasing voltages is shown in Fig. (1). All measurements have been carried out inside a black box at room temperature. It is clear that the resistivity is decreased when the substrate temperature increased up to (170 °C), then increased as (Ts) become more than (170 °C). The decreasing in resistivity at substrate temperature less than(170 °C) is due to the sensitivity of the grain size to the substrate temperature and it grows exponentially as a function of (Ts).This increase in grain size (decrease in barriers) as the function of (Ts) is a consequence of the larger mobility of the atoms at high temperature for both CdS and CdTe (Mohammad and Nory, 1997 and Hussain, 1992). Other researchers reported that the increasing in the substrate temperature causes an increase in the grain size (Mohammad, 2003) and (Ramadan, 1992).

The increasing in resistivity at substrate temperature higher than (170 °C) could be explained as follows : **first,** the degree of preferential orientation of the micro crystallites becomes less as (Ts) increases (Ashor et al., 1994). Since it is known that there is a positive correlation between the degree of preferential orientation and the conductivity ($\sigma = 1/\rho$) .**second**, at high (Ts) the adhesion coefficient of Cd (donor) is small, therefore the (CdS –CdTe) thin films becomes rich in (S) and (Te) atoms (acceptors). In other words, at (Ts) higher than (170 °C) some of the evaporated atoms (specially Cd atoms) start to rebounds (re – evaporates) from the substrate causing an increase in resistivity because the thin films will have dielectric properties more than conduction properties (Nory, 1995) and (Mohammad, 1995).

Also, from Fig.(1), it is clear that the bulk resistivity decreased with increasing the biasing voltage because the voltage drop in the barrier becomes less (according to Eq. 1).

Fig.(2) shows the bulk current – voltage (I-V) characteristics for different substrate temperatures . It is clear that the current is directly related with the voltage and increases with the substrate temperature up to (170 °C) then starts to decrease as (Ts) becomes more than (170 °C) . This is because the current is inversely related with the resistivity according to Ohms law . The optimum substrate temperature (170 °C) has a maximum current .

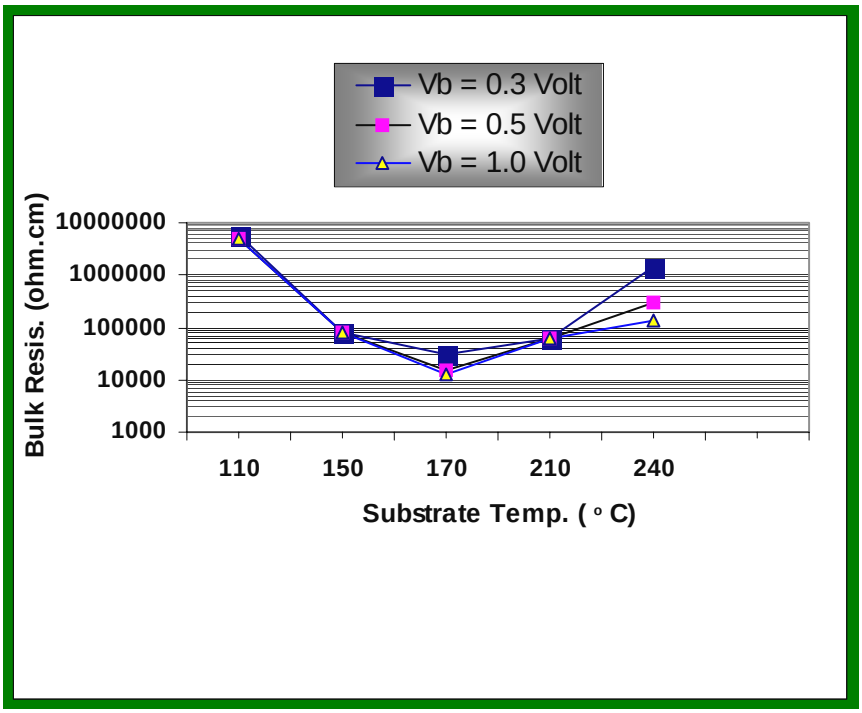

Fig. 1: Variation of bulk resistivity with substrate temperature for different Biasing voltages (Vb) .

Fig.(3) illustrates the variation of surface resistivity (ρ_s) against the substrate Temp. for two values of biasing voltages (5V & 10V). It is clear that the behavior and analysis of these curves are similar to the curves shown in figure (1) for (Ts) range (110 °C - 170 °C). It is worth mentioning that the calculating of surface resistivity follows this equation (Nory , 1995) :

$$\rho_s = \frac{R \cdot A}{L} \quad \text{..... (2)}$$

Where ($R = V_b / I$) and V_b , A , & L represents the biasing voltage, area of the contacts, and the distance between electrodes respectively. The area of contacts may be determined by knowing the thickness of thin film layer and the length of contact layer (electrode). While the calculating of bulk resistivity follows the same equation above but (L) equal to the thickness of (CdS - CdTe) thin film and (A) equal to the aluminum layer length multiplexing by its width.

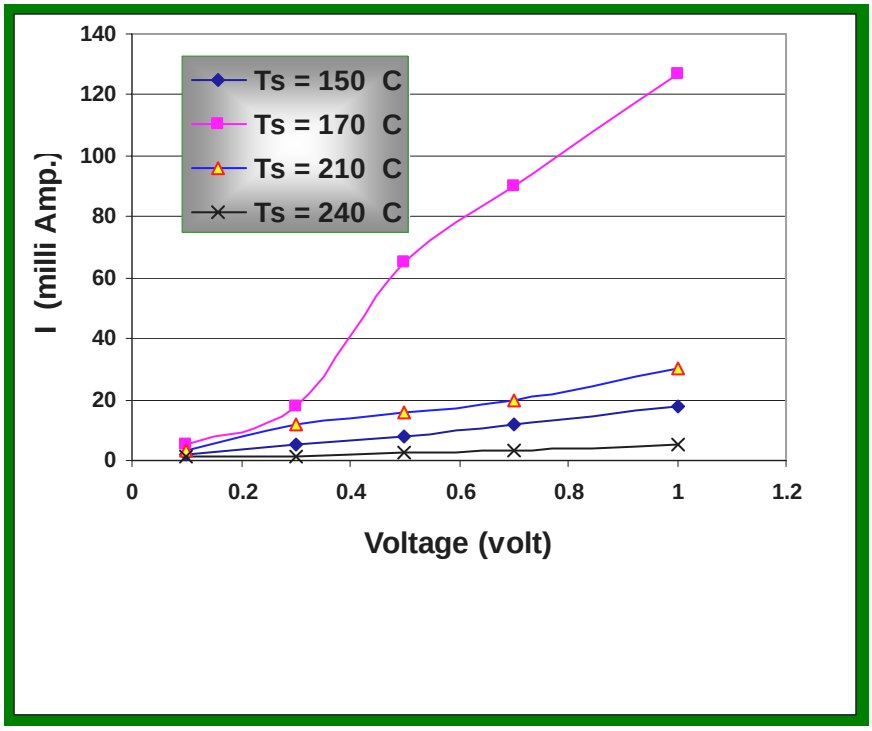

Fig. 2: (I-V) Characteristics for different substrate temperatures (Ts).

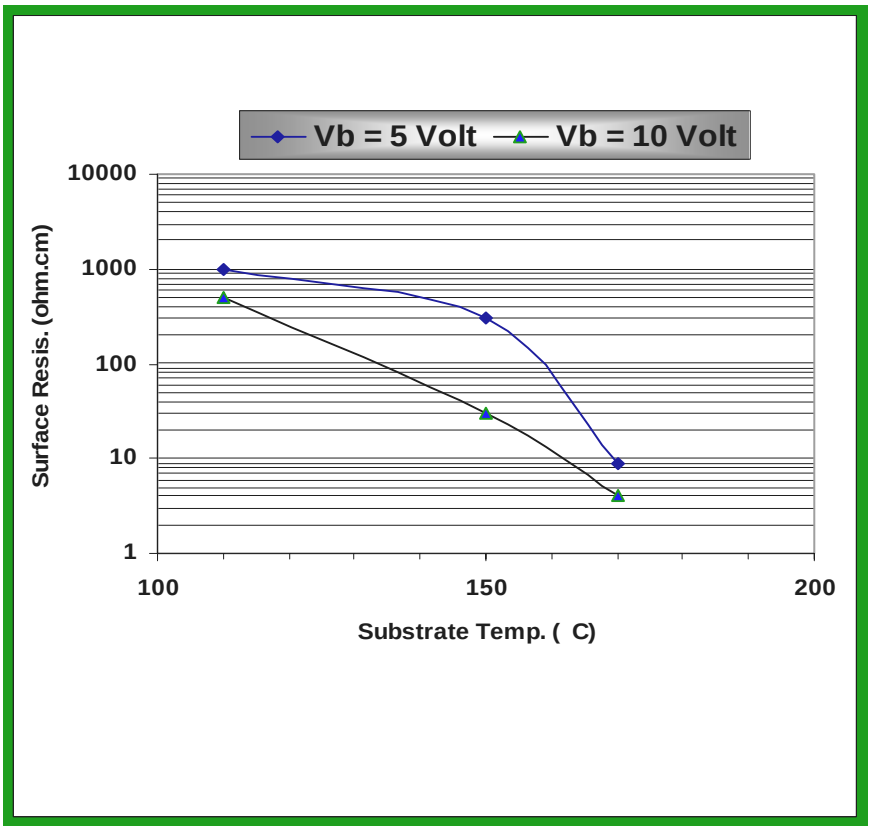

Fig. 3: Variation of surface resistivity (ρ_s) with substrate temperature (Ts) for two values of biasing voltages (Vb) .

The dependence of bulk current on the substrate Temp. for variable biasing voltages is shown in Fig.(4). It is obvious that the curves have maximum points at (Ts) equal to (170 °C) and the current increases with increasing the biasing voltage. The behavior of these curves is the inverse of the curves in figure (1) according to the equation below (Hussain, 1992) :

$$\rho = \frac{V_b \cdot A}{I \cdot L} \qquad (3)$$

By substituting Eq.1 in Eq.3, the relation of grain size (which is affected by substrate Temp.) with the current, follows the equation below (Nory, 1995) :

$$I = \frac{V_b \cdot A \cdot D \cdot J}{V \cdot L} \qquad (4)$$

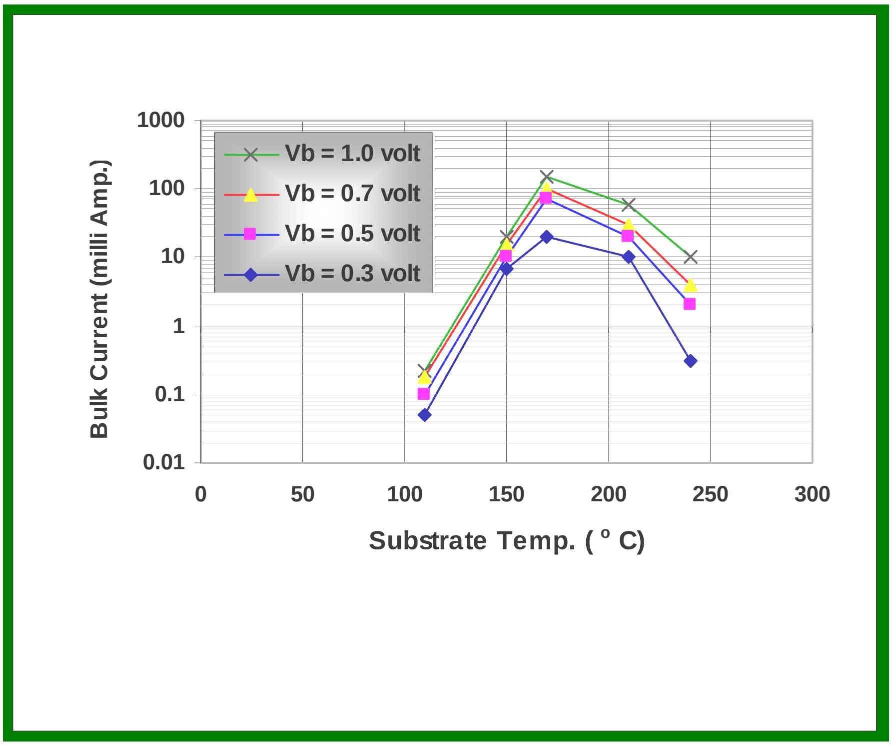

Fig. 4: Variation of bulk current (Ib) with substrate temperature (Ts) for different biasing voltages (Vb) .

Fig. (5) represents the variation of surface resistivity with the biasing voltage for different substrate temperature. It is clear that the resistivity is decreased with increasing the biasing voltage according to the above equation (4). Also, it is observed that the resistivity is inversely proportional with the substrate Temp.

A comparison between the diffraction patterns of (CdS – CdTe) powder and the film which fabricated at (Ts=170 °C) is shown in Fig. (6), which implies that the polycrystalline films are preferentially oriented. (002) reflections is considerably more intense than all other reflections. Hence the c-axis is normal to the substrate surface corresponding to the (001) fiber texture.

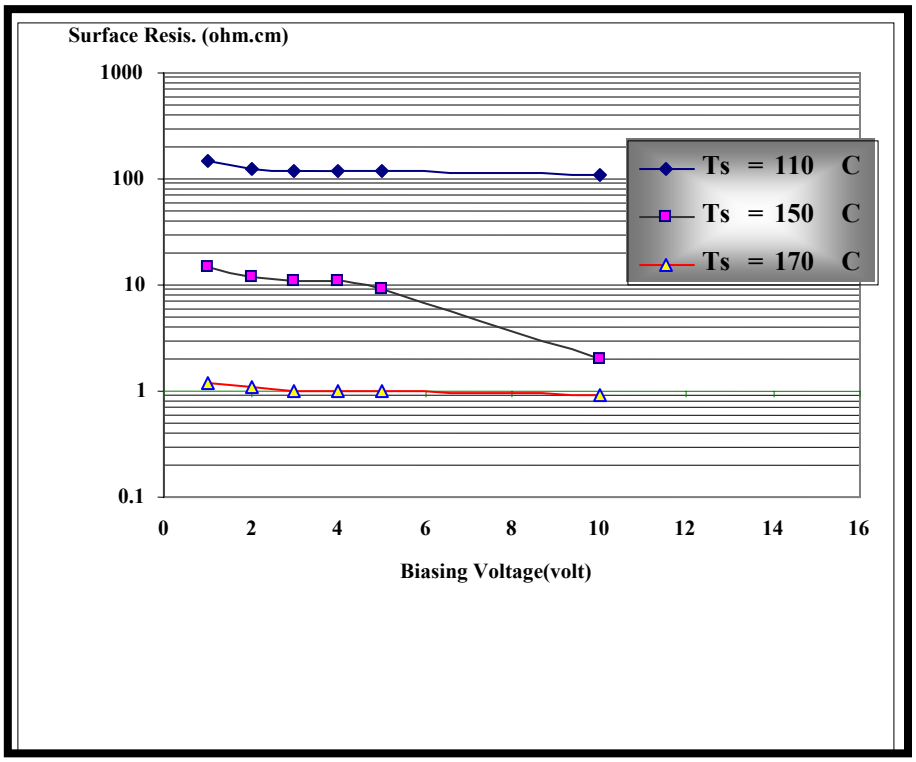

Fig. 5: Variation of surface resistivity (ρ_s) with biasing voltage (Vb) for Different substrate temperatures (Ts).

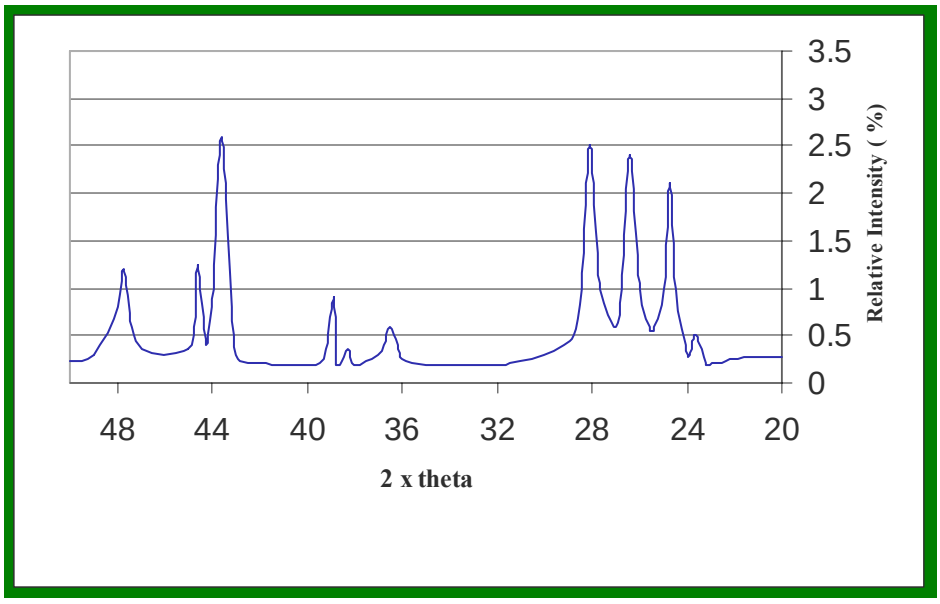

Fig. 6-a: X-ray diffractometer traces obtained from (CdS+CdTe) powder.

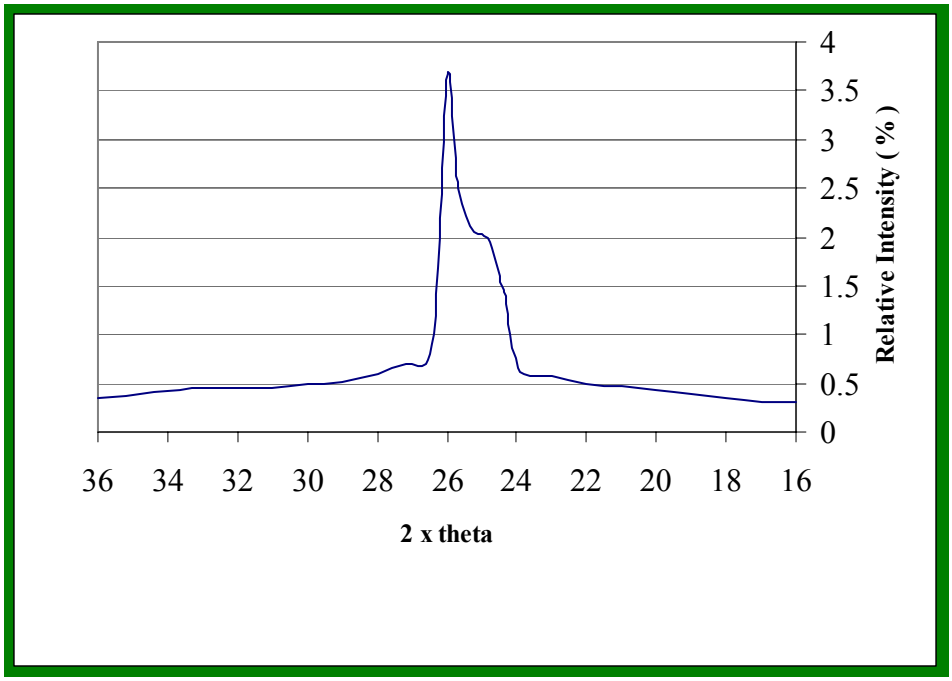

Fig. 6-b: X-ray diffractometer traces obtained from (CdS+CdTe) thin film with (Ts = 170 °C) .

CONCLUSIONS

The electrical resistivity of (CdS - CdTe) mixture thin films depends very strongly on the substrate temperature. The optimum resistivity can be obtained by choosing substrate temperature equal to (170 °C) which is suitable for the practical applications . The [AL – (CdS – CdTe)] contacts were ohmic one. The maximum bulk current obtained is (154) mA at (Ts =170 °C). The film which deposited at (Ts =170 °C) was found to be highly oriented with the hexagonal C – axis perpendicular to the substrate and the CdS semiconductor at (002) direction was the dominant orientation with the structure.

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